

REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 1-28 are pending and Claims 13-28 are withdrawn. Claims 1-12 are rejected and Claims 1, 5, and 9 are amended hereinabove.

Independent Claim 1 positively recites performing a supplemental isolation implant within at least one of the first type well regions of the embedded transistor-containing memory portion to modify dopant profile(s) of the at least one of the first type well regions to increase isolation. These advantageously claimed features are not taught or suggested by the patent granted to Dennison.

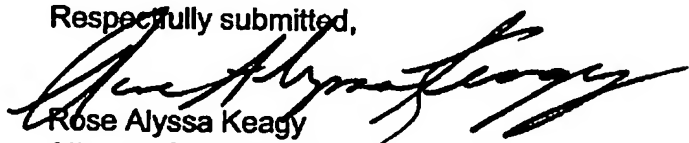
Dennison does not teach the advantageously claimed invention because Dennison only teaches the use of phase-change memory elements - which by definition are void of transistors (column 3 lines 23-24); but not the use of transistor-containing memory portions as advantageously claimed (reference the Applicants' FIGS. 5-9, 11-14, and 17-20).

The Applicants respectfully traverse the statements in the Office Action (pages 3-4) that Dennison teaches the use of different shallow trench isolation widths in columns 6-7 lines 55-45 (where alternative memory array structures (i.e. element 102) are discussed – see column 7 lines 3-4). The Applicants respectfully submit that Dennison does not teach the use of different shallow trench isolation widths (column 4 lines 34-35, FIGS. 2-6).

For the foregoing reasons, the Applicants respectfully traverse the rejection of Claim 1 and respectfully assert that Claim 1 is patentable over the patent granted to Dennison. Furthermore, Claims 2-12 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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